What is claimed is:

1. A semiconductor device of high breakdown voltage comprising:

a gate electrode pattern embedded in an active area of a semiconductor substrate, which area is defined by a device separating film having an inversion preventing layer;

a gate insulating layer pattern surrounding the gate electrode pattern;

high concentration impurity layers located on both sides of the gate electrode pattern to contact the gate insulating layer pattern and formed in an upper layer of the active area of the semiconductor substrate by an ion implantation; and

low concentration impurity layers located on both sides of the gate electrode pattern to contact the gate insulating layer pattern and formed under the high concentration impurity layers by an ion implantation.

2. The device according to claim 1, wherein the high concentration impurity layers are separately formed so as not to electrically contact the inversion preventing layer of the

device separating film.

3. The device according to claim 1, wherein junctions of the low concentration impurity layers are formed at a depth equal to or deeper than the depth of the embedded gate electrode pattern by the ion-implantation.

4. The device according to claim 1, wherein the gate electrode pattern is embedded in a depth shallower than the device separating film.

5. The device according to claim 1, wherein the gate electrode pattern maintains a width wider than the device separating film.

6. The device according to claim 1, further comprising a threshold voltage control layer provided in a bottom of the gate insulating layer pattern for controlling a threshold voltage of a channel formed by the gate insulating layer pattern.

7. A method of manufacturing a semiconductor

device of high breakdown voltage comprising steps of:

forming a trench in an active area of a semiconductor substrate;

forming a gate insulating layer pattern on a surface of the trench;

forming a gate electrode pattern in the trench to contact the gate insulating layer pattern;

forming low concentration impurity layers in the active area of the semiconductor substrate to contact the gate insulating layer pattern and to be located on both sides of the gate electrode pattern by an ion implantation; and

forming high concentration impurity layers on the low concentration impurity layers to contact the gate insulating layer pattern and to be located on both sides of the gate electrode pattern by an ion implantation.

8. The method according to claim 7, further comprising a step of forming a threshold voltage control layer in a bottom of the gate insulating layer pattern for controlling a threshold voltage of a channel formed by the gate insulating layer pattern.

9. The method according to claim 7, wherein the gate insulating layer pattern is formed to have a thickness of 180Å~2500Å.

10. The method according to claim 7, further comprising a step of driving-in the low concentration impurity layers at high temperatures.

11. The method according to claim 10, wherein the step of driving-in the low concentration impurity layers is performed at 1000°C~1250°C.

12. The method according to claim 10, wherein the step of driving-in the low concentration impurity layers is performed for 30 min.~ 600 min.